MCP3905/06

Energy-Metering ICs with Active (Real) Power Pulse Output

Features

- Supplies active (real) power measurement for single-phase, residential energy-metering
- Supports the IEC 62053 International Energy Metering Specification and legacy IEC 1036/61036/687 Specifications
- Two multi-bit, Digital-to-Analog Converters (DACs), second-order, 16-bit, Delta-Sigma Analog-to-Digital Converters (ADCs)
- 0.1% typical measurement error over **500:1** dynamic range **(MCP3905)**
- 0.1% typical measurement error over **1000:1** dynamic range **(MCP3906)**
- Programmable Gain Amplifier (PGA) for small-signal inputs supports low-value shunt current sensor
  - **16:1** PGA - **MCP3905**
  - **32:1** PGA - **MCP3906**
- Ultra-low drift on-chip reference: 15 ppm/°C (typ.)
- Direct drive for electromagnetic mechanical counter and two-phase stepper motors
- Low I_{DD} of 4 mA (typ.)
- Tamper output pin for negative power indication
- Industrial Temperature Range: -40°C to +85°C
- Supplies instantaneous active (real) power on HF_{OUT} for meter calibration

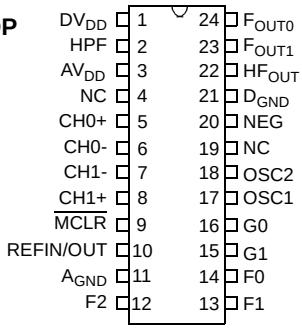
US Patents Pending

Description

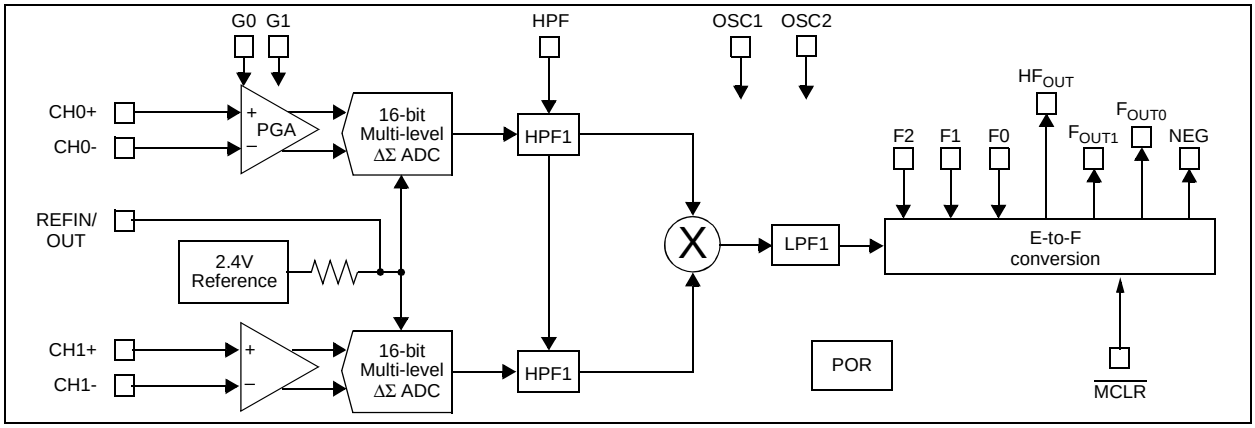
The MCP3905/06 devices are energy-metering ICs designed to support the IEC 62053 International Metering Standard Specification. They supply a frequency output proportional to the average active (real) power, as well as a higher-frequency output proportional to the instantaneous power for meter calibration. They include two 16-bit, delta-sigma ADCs for a wide range of I_B and I_{MAX} currents and/or small shunt (< 200 µOhms) meter designs. It includes an ultra-low drift voltage reference with < 15 ppm/°C through a specially designed band gap temperature curve for the minimum gradient across the industrial temperature range. A fixed-function DSP block is on-chip for active (real) power calculation. Strong output drive for mechanical counters are on-chip to reduce field failures and mechanical counter sticking. A no-load threshold block prevents any current creep measurements. A Power-On Reset (POR) block restricts meter performance during low-voltage situations. These accurate energy-metering ICs with high field reliability are available in the industry-standard pinout.

Package Type

24-Pin SSOP



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} 7.0V
Digital inputs and outputs w.r.t. A_{GND}..... -0.6V to V_{DD} +0.6V
Analog input w.r.t. A_{GND} .....-6V to +6V
V_{REF} input w.r.t. A_{GND} ..... -0.6V to V_{DD} +0.6V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) .....5.0 kV, 500V
ESD on all other pins (HBM,MM) .....5.0 kV, 500V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at $AV_{DD} = DV_{DD} = 4.5V – 5.5V$, Internal V_{REF}, HPF turned on (AC mode), A_{GND}, D_{GND} = 0V, MCLK = 3.58 MHz; T_A = -40°C to +85°C.

Parameter	Sym	Min	Typ.	Max	Units	Comment
Overall Measurement Accuracy						
Energy Measurement Error	E	—	0.1	—	% F_{OUT}	Channel 0 swings 1:500 range, MCP3905 only (**Note 1**, **Note 4**)
		—	0.1	—	% F_{OUT}	Channel 0 swings 1:1000 range, MCP3906 only (**Note 1**, **Note 4**)
No-Load Threshold/ Minimum Load	NLT	—	0.0015	—	% F_{OUT} Max	Disabled when F2, F1, F0 = 0, 1, 1 (**Note 5, Note 6**)
Phase Delay Between Channels		—	—	1/MCLK	s	HPF = 0 and 1, < 1 MCLK (**Note 4, Note 6, Note 7**)
AC Power Supply Rejection Ratio (Output Frequency Variation)	AC PSRR	—	0.01	—	% F_{OUT}	F2, F1, F0 = 0, 1, 1 (**Note 3**)
DC Power Supply Rejection Ratio (Output Frequency Variation)	DC PSRR	—	0.01	—	% F_{OUT}	HPF = 1, Gain = 1 (**Note 3**)
System Gain Error		—	3	10	% F_{OUT}	**Note 2, Note 5**
ADC/PGA Specifications						
Offset Error	V_{OS}	—	2	5	mV	Referred to Input
Gain Error Match		—	0.5	—	% F_{OUT}	**Note 8**
Internal Voltage Reference						
Voltage		—	2.4	—	V	
Tolerance		—	±2	—	%	
Tempco		—	15	—	ppm/°C	

Note 1: Measurement error = (Energy Measured By Device - True Energy)/True Energy * 100%. Accuracy is measured with signal (±660 mV) on Channel 1. F_{OUT0}, F_{OUT1} pulse outputs. Valid from 45 Hz to 65 Hz. See **Section 2.0 "Typical Performance Curves"** for higher frequencies and increased dynamic range.

2: Does not include internal V_{REF}. Gain = 1, CH0 = 470 mVDC, CH1 = 660 mVDC, difference between measured output frequency and expected transfer function.

3: Percent of HF_{OUT} output frequency variation; Includes external V_{REF} = 2.5V, CH1 = 100 mVRMS @ 50 Hz, CH2 = 100 mVRMS @ 50 Hz, AV_{DD} = 5V + $1V_{pp}$ @ 100 Hz. DC PSRR: 5V ±500 mV.

4: Error applies down to 60° lead (PF = 0.5 capacitive) and 60° lag (PF = 0.5 inductive).

5: Refer to **Section 4.0 "Device Overview"** for complete description.

6: Specified by characterization, not production tested.

7: 1 MCLK period at 3.58 MHz is equivalent to less than <0.005 degrees at 50 or 60 Hz.

8: Gain error match is measured from CH0 G = 1 to any other gain setting.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 4.5V – 5.5V, Internal V_{REF}, HPF turned on (AC mode), A_{GND}, D_{GND} = 0V, MCLK = 3.58 MHz; T_A = -40°C to +85°C.

Parameter	Sym	Min	Typ.	Max	Units	Comment
Reference Input						
Input Range		2.2	—	2.6	V	
Input Impedance		3.2	—	—	kΩ	
Input Capacitance		—	—	10	pF	
Analog Inputs						
Maximum Signal Level		—	—	±1	V	CH0+,CH0-,CH1+,CH1- to A_{GND}
Differential Input Voltage Range Channel 0		—	—	±470/G	mV	G = PGA Gain on Channel 0
Differential Input Voltage Range Channel 1		—	—	±660	mV	
Input Impedance		390	—	—	kΩ	Proportional to 1/MCLK frequency
Bandwidth (Notch Frequency)		—	14	—	kHz	Proportional to MCLK frequency, MCLK/256
Oscillator Input						
Frequency Range	MCLK	1	—	4	MHz	
Power Specifications						
Operating Voltage		4.5	—	5.5	V	AV_{DD}, DV_{DD}
$I_{DD,A}$	$I_{DD,A}$	—	2.7	3.0	mA	AV_{DD} pin only
$I_{DD,D}$	$I_{DD,D}$	—	1.2	2.0	mA	DV_{DD} pin only

Note 1: Measurement error = (Energy Measured By Device - True Energy)/True Energy * 100%. Accuracy is measured with signal (±660 mV) on Channel 1. F_{OUT0}, F_{OUT1} pulse outputs. Valid from 45 Hz to 65 Hz. See **Section 2.0 "Typical Performance Curves"** for higher frequencies and increased dynamic range.

2: Does not include internal V_{REF}. Gain = 1, CH0 = 470 mVDC, CH1 = 660 mVDC, difference between measured output frequency and expected transfer function.

3: Percent of HF_{OUT} output frequency variation; Includes external V_{REF} = 2.5V, CH1 = 100 mVRMS @ 50 Hz, CH2 = 100 mVRMS @ 50 Hz, AV_{DD} = 5V + $1V_{pp}$ @ 100 Hz. DC PSRR: 5V ±500 mV.

4: Error applies down to 60° lead (PF = 0.5 capacitive) and 60° lag (PF = 0.5 inductive).

5: Refer to **Section 4.0 "Device Overview"** for complete description.

6: Specified by characterization, not production tested.

7: 1 MCLK period at 3.58 MHz is equivalent to less than <0.005 degrees at 50 or 60 Hz.

8: Gain error match is measured from CH0 G = 1 to any other gain setting.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 4.5V – 5.5V, A_{GND}, D_{GND} = 0V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	

Note: The MCP3905/06 operate over this extended temperature range, but with reduced performance. In any case, the Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

TIMING CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 4.5V – 5.5V, A_{GND}, D_{GND} = 0V, MCLK = 3.58 MHz; T_A = -40°C to +85°C.

Parameter	Sym	Min	Typ	Max	Units	Comment
Frequency Output						
F_{OUT0} and F_{OUT1} Pulse Width (Logic-Low)	t_{FW}	—	275	—	ms	984376 MCLK periods **(Note 1)**
HF_{OUT} Pulse Width	t_{HW}	—	90	—	ms	322160 MCLK periods **(Note 2)**
F_{OUT0} and F_{OUT1} Pulse Period	t_{FP}	Refer to Equation 4-1			s	
HF_{OUT} Pulse Period	t_{HP}	Refer to Equation 4-2			s	
F_{OUT0} to F_{OUT1} Falling-Edge Time	t_{FS2}	—	0.5 t_{FP}	—		
F_{OUT0} to F_{OUT1} Min Separation	t_{FS}	—	4/MCLK	—		
F_{OUT0} and F_{OUT1} Output High Voltage	V_{OH}	4.5	—	—	V	I_{OH} = 10 mA, DV_{DD} = 5.0V
F_{OUT0} and F_{OUT1} Output Low Voltage	V_{OL}	—	—	0.5	V	I_{OL} = 10 mA, DV_{DD} = 5.0V
HF_{OUT} Output High Voltage	V_{OH}	4.0	—	—	V	I_{OH} = 5 mA, DV_{DD} = 5.0V
HF_{OUT} Output Low Voltage	V_{OL}	—	—	0.5	V	I_{OL} = 5 mA, DV_{DD} = 5.0V
High-Level Input Voltage (All Digital Input Pins)	V_{IH}	2.4	—	—	V	DV_{DD} = 5.0V
Low-Level Input Voltage (All Digital Input Pins)	V_{IL}	—	—	0.85	V	DV_{DD} = 5.0V
Input Leakage Current		—	—	±3	µA	V_{IN} = 0, V_{IN} = DV_{DD}
Pin Capacitance		—	—	10	pF	**Note 3**

Note 1: If output pulse period (t_{FP}) falls below 984376*2 MCLK periods, then t_{FW} = 1/2 t_{FP}.

2: If output pulse period (t_{HP}) falls below 322160*2 MCLK periods, then t_{HW} = 1/2 t_{HP}.

3: Specified by characterization, not production tested.

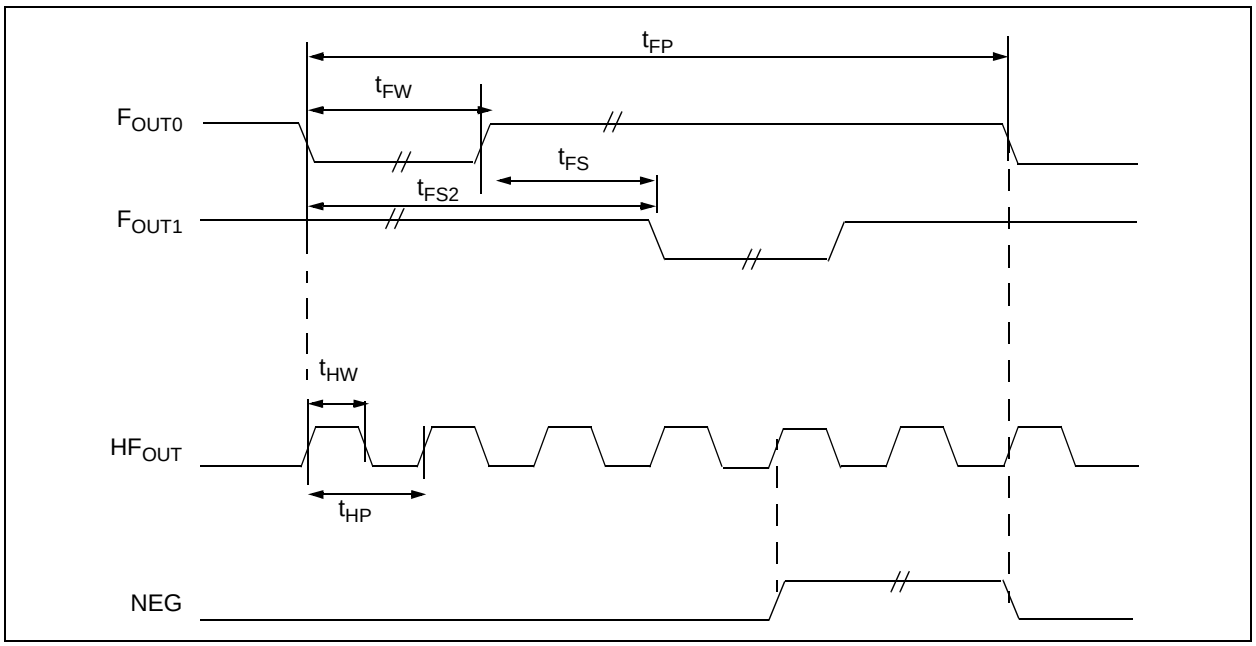


FIGURE 1-1: *Output Timings for Pulse Outputs and Negative Power Pin.*

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, DV_{DD}, AV_{DD} = 5V; A_{GND}, D_{GND} = 0V; V_{REF} = Internal, HPF = 1 (AC mode), MCLK = 3.58 MHz.

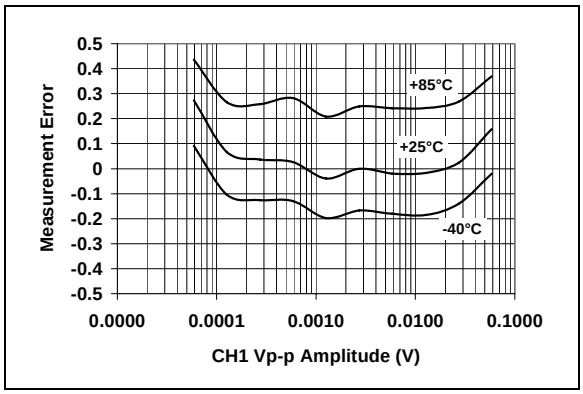


FIGURE 2-1: *Measurement Error, Gain = 8, PF = 1.*

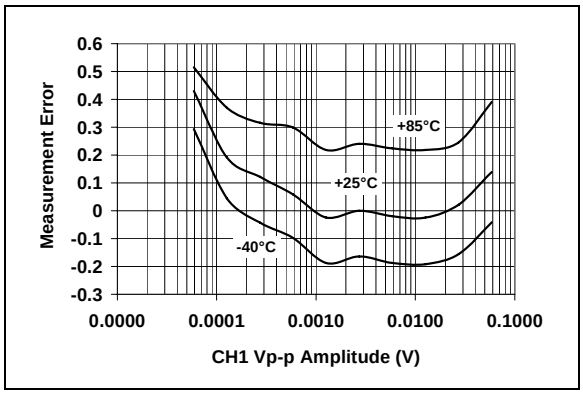


FIGURE 2-4: *Measurement Error, Gain = 8, PF = 0.5.*

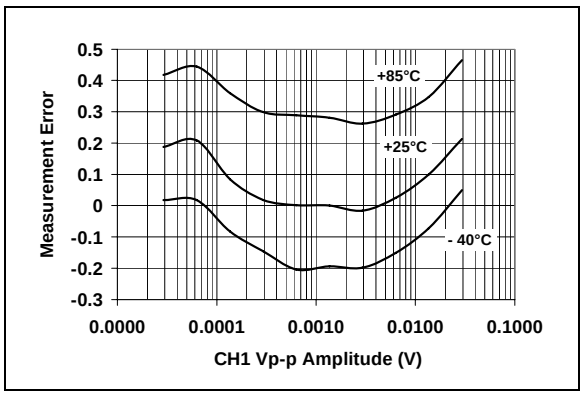


FIGURE 2-2: *Measurement Error, Gain = 16, PF = 1.*

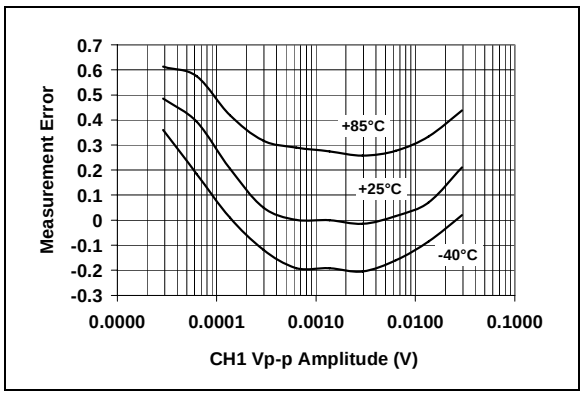


FIGURE 2-5: *Measurement Error, Gain = 16, PF = 0.5.*

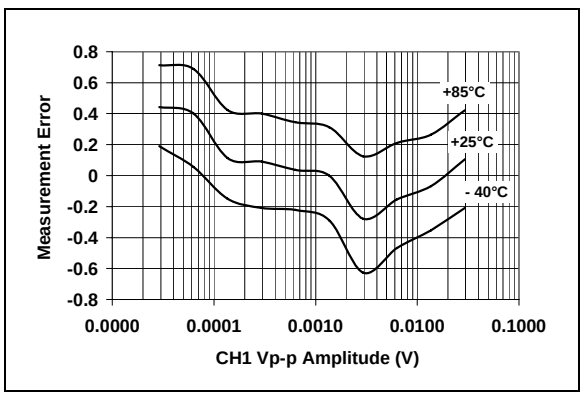


FIGURE 2-3: *Measurement Error, Gain = 32, PF = 1.*

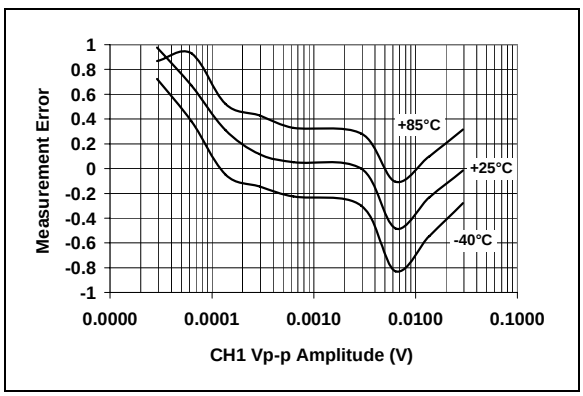


FIGURE 2-6: *Measurement Error, Gain = 32, PF = 0.5.*

Note: Unless otherwise specified, DV_{DD}, AV_{DD} = 5V; A_{GND}, D_{GND} = 0V; V_{REF} = Internal, HPF = 1 (AC mode), MCLK = 3.58 MHz.

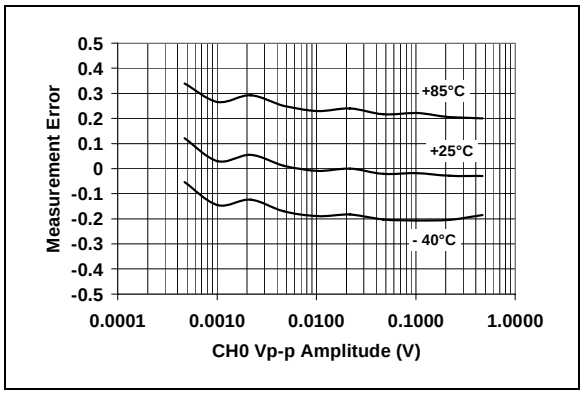


FIGURE 2-7: *Measurement Error, Gain = 1, PF = 1.*

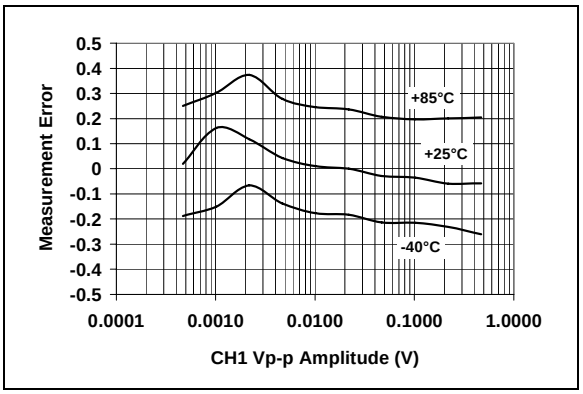


FIGURE 2-9: *Measurement Error, Gain = 1, PF = + 0.5.*

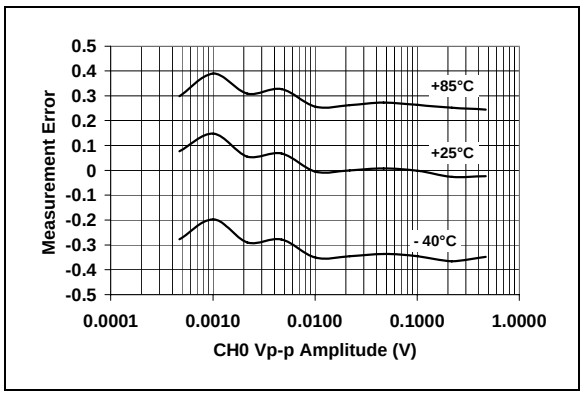


FIGURE 2-8: *Measurement Error, Gain = 2, PF = 1.*

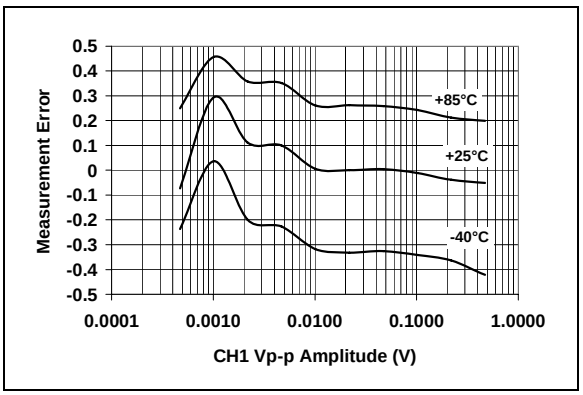


FIGURE 2-10: *Measurement Error, Gain = 2, PF = + 0.5.*

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Note: Unless otherwise specified, DV_{DD}, AV_{DD} = 5V; A_{GND}, D_{GND} = 0V; V_{REF} = Internal, HPF = 1 (AC mode), MCLK = 3.58 MHz.

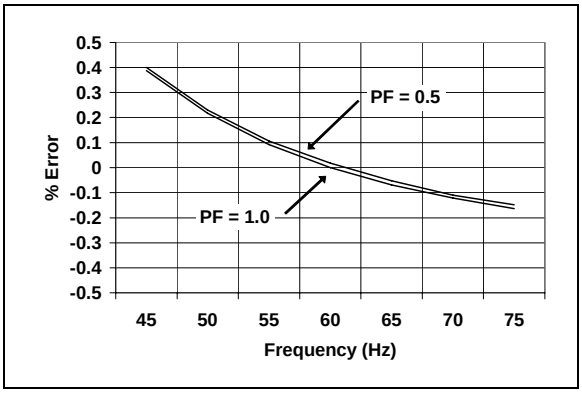


FIGURE 2-11: *Measurement Error vs. Input Frequency.*

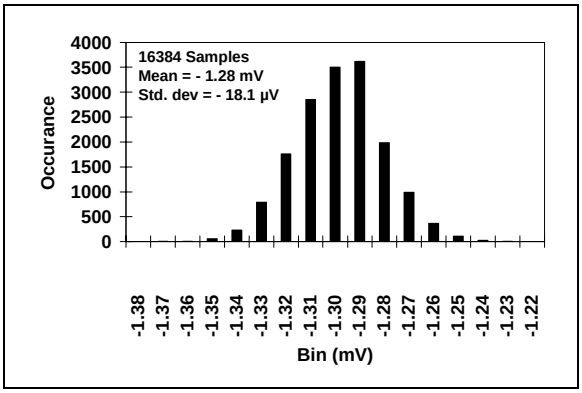


FIGURE 2-14: *Channel 0 Offset Error (DC Mode, HPF Off), G = 16.*

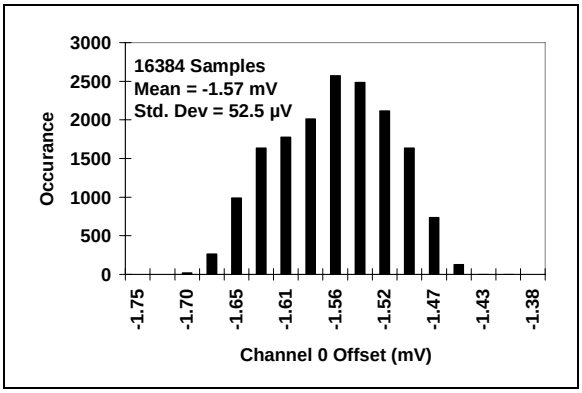


FIGURE 2-12: *Channel 0 Offset Error (DC Mode, HPF off), G = 1.*

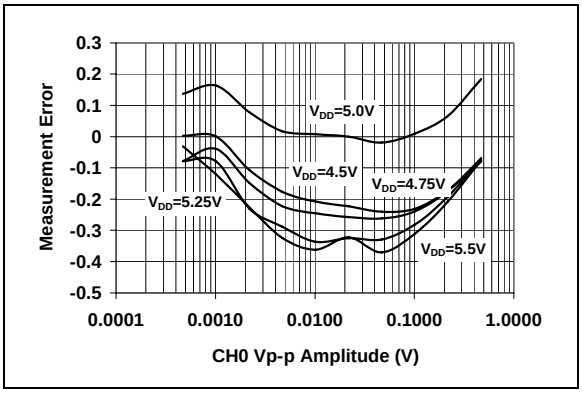


FIGURE 2-15: *Measurement Error vs. V_{DD} (G = 16).*

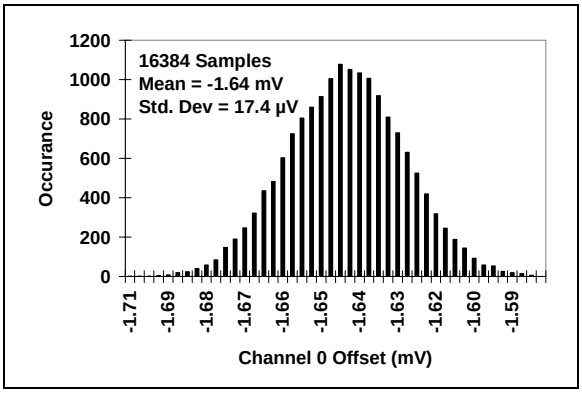


FIGURE 2-13: *Channel 0 Offset Error (DC Mode, HPF off), G = 8.*

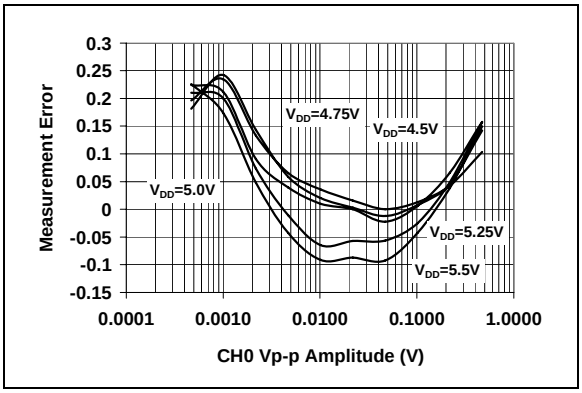


FIGURE 2-16: *Measurement Error vs. V_{DD}, G = 16, External V_{REF}.*

Note: Unless otherwise specified, DV_{DD}, AV_{DD} = 5V; A_{GND}, D_{GND} = 0V; V_{REF} = Internal, HPF = 1 (AC mode), MCLK = 3.58 MHz.

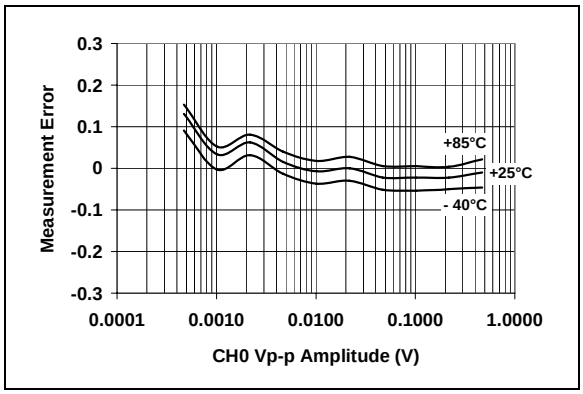


FIGURE 2-17: *Measurement Error w/ External V_{REF}, (G = 1).*

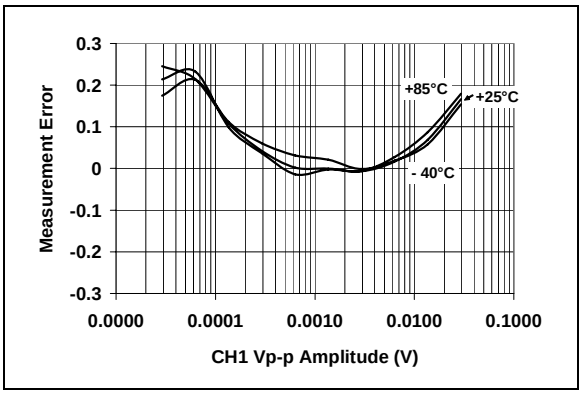


FIGURE 2-19: *Measurement Error w/ External V_{REF} (G = 16).*

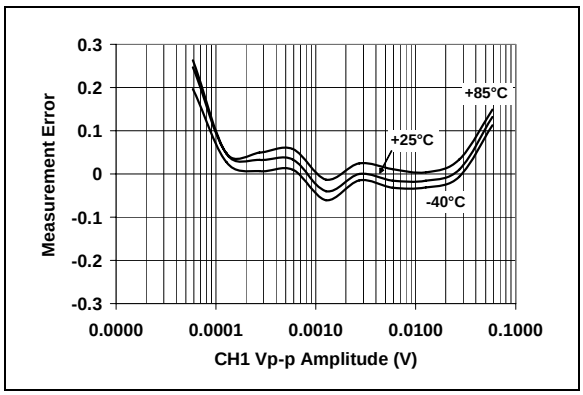


FIGURE 2-18: *Measurement Error w/ External V_{REF}, (G = 8).*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	Symbol	Function
1	DV_{DD}	Digital Power Supply Pin
2	HPF	High-Pass Filters Control Logic Pin
3	AV_{DD}	Analog Power Supply Pin
4	NC	No Connect
5	CH0+	Non-Inverting Analog Input Pin for Channel 0 (Current Channel)
6	CH0-	Inverting Analog Input Pin for Channel 0 (Current Channel)
7	CH1-	Inverting Analog Input Pin for Channel 1 (Voltage Channel)
8	CH1+	Non-Inverting Analog Input Pin for Channel 1 (Voltage Channel)
9	$\overline{MCLR}$	Master Clear Logic Input Pin
10	REFIN/OUT	Voltage Reference Input/Output Pin
11	A_{GND}	Analog Ground Pin, Return Path for internal analog circuitry
12	F2	Frequency Control for HF_{OUT} Logic Input Pin
13	F1	Frequency Control for $F_{OUT0/1}$ Logic Input Pin
14	F0	Frequency Control for $F_{OUT0/1}$ Logic Input Pin
15	G1	Gain Control Logic Input Pin
16	G0	Gain Control Logic Input Pin
17	OSC1	Oscillator Crystal Connection Pin or Clock Input Pin
18	OSC2	Oscillator Crystal Connection Pin or Clock Output Pin
19	NC	No Connect
20	NEG	Negative Power Logic Output Pin
21	D_{GND}	Digital Ground Pin, Return Path for Internal Digital Circuitry
22	HF_{OUT}	High-Frequency Logic Output Pin (Intended for Calibration)
23	F_{OUT1}	Differential Mechanical Counter Logic Output Pin
24	F_{OUT0}	Differential Mechanical Counter Logic Output Pin

3.1 Digital V_{DD} (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP3905/06.

DV_{DD} requires appropriate bypass capacitors and should be maintained to 5V ±10% for specified operation. Please refer to **Section 5.0 "Applications Information"**.

3.2 High-Pass Filter Input Logic Pin (HPF)

HPF controls the state of the high-pass filter in both input channels. A logic '1' enables both filters, removing any DC offset coming from the system or the device. A logic '0' disables both filters, allowing DC voltages to be measured.

3.3 Analog V_{DD} (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP3905/06.

AV_{DD} requires appropriate bypass capacitors and should be maintained to 5V ±10% for specified operation. Please refer to **Section 5.0 "Applications Information"**.

3.4 Current Channel (CH0-, CH0+)

CH0- and CH0+ are the fully differential analog voltage input channels for the current measurement, containing a PGA for small-signal input, such as shunt current-sensing. The linear and specified region of this channel is dependant on the PGA gain. This corresponds to a maximum differential voltage of ±470 mV/GAIN and maximum absolute voltage, with respect to A_{GND}, of ±1V. Up to ±6V can be applied to these pins without the risk of permanent damage.

Refer to **Section 1.0 "Electrical Characteristics"**.

3.5 Voltage Channel (CH1-,CH1+)

CH1- and CH1+ are the fully differential analog voltage input channels for the voltage measurement. The linear and specified region of these channels have a maximum differential voltage of ±660mV and a maximum absolute voltage of ±1V, with respect to A_{GND}. Up to ±6V can be applied to these pins without the risk of permanent damage.

Refer to **Section 1.0 "Electrical Characteristics"**.

3.6 Master Clear ($\overline{MCLR}$)

$\overline{MCLR}$ controls the reset for both delta-sigma ADCs, all digital registers, the SINC filters for each channel and all accumulators post multiplier. A logic '0' resets all registers and holds both ADCs in a Reset condition. The charge stored in both ADCs is flushed and their output is maintained to 0x0000h. The only block consuming power on the digital power supply during Reset is the oscillator circuit.

3.7 Reference (REFIN/OUT)

REFIN/OUT is the output for the internal 2.4V reference. This reference has a typical temperature coefficient of 15 ppm/°C and a tolerance of ±2%. In addition, an external reference can also be used by applying voltage to this pin within the specified range. REFIN/OUT requires appropriate bypass capacitors to A_{GND}, even when using the internal reference only. Refer to **Section 5.0 "Applications Information"**.

3.8 Analog Ground (A_{GND})

A_{GND} is the ground connection to the internal analog circuitry (ADCs, PGA, band gap reference, POR). To ensure accuracy and noise cancellation, this pin must be connected to the same ground as D_{GND}, preferably with a star connection. If an analog ground plane is available, it is recommended that this device be tied to this plane of the Printed Circuit Board (PCB). This plane should also reference all other analog circuitry in the system.

3.9 Frequency Control Logic Pins (F2, F1, F0)

F2, F1 and F0 select the high-frequency output and low-frequency output pin ranges by changing the value of the constants F_C and H_{FC} used in the device transfer function. F_C and H_{FC} are the frequency constants that define the period of the output pulses for the device.

3.10 Gain Control Logic Pins (G1, G0)

G1 and G0 select the PGA gain on Channel 0 from three different values: 1, 8 and 16.

3.11 Oscillator (OSC1, OSC2)

OSC1 and OSC2 provide the master clock for the device. A resonant crystal or clock source with a similar sinusoidal waveform must be placed across these pins to ensure proper operation. The typical clock frequency specified is 3.579545 MHz. However, the clock frequency can be with the range of 1 MHz to 4 MHz without disturbing measurement error. Appropriate load capacitance should be connected to these pins for proper operation.

A full-swing, single-ended clock source may be connected to OSC1 with proper resistors in series to ensure no ringing of the clock source due to fast transient edges.

3.12 Negative Power Output Logic Pin (NEG)

NEG detects the phase difference between the two channels and will go to a logic '1' state when the phase difference is greater than 90° (i.e., when the measured active (real) power is negative). The output state is synchronous with the rising-edge of HF_{OUT} and maintains the logic '1' until the active (real) power becomes positive again and HF_{OUT} shows a pulse.

3.13 Ground Connection (D_{GND})

D_{GND} is the ground connection to the internal digital circuitry (SINC filters, multiplier, HPF, LPF, Digital-to-Frequency (DTF) converter and oscillator). To ensure accuracy and noise cancellation, D_{GND} must be connected to the same ground as A_{GND}, preferably with a star connection. If a digital ground plane is available, it is recommended that this device be tied to this plane of the PCB. This plane should also reference all other digital circuitry in the system.

3.14 High-Frequency Output (HF_{OUT})

HF_{OUT} is the high-frequency output of the device and supplies the instantaneous real-power information. The output is a periodic pulse output, with its period proportional to the measured active (real) power, and to the HF_C constant defined by F0, F1 and F2 pin logic states. This output is the preferred output for calibration due to faster output frequencies, giving smaller calibration times. Since this output gives instantaneous active (real) power, the 2ω ripple on the output should be noted. However, the average period will show minimal drift.

3.15 Frequency Output (F_{OUT0}, F_{OUT1})

F_{OUT0} and F_{OUT1} are the frequency outputs of the device that supply the average real-power information. The outputs are periodic pulse outputs, with its period proportional to the measured active (real) power, and to the F_c constant, defined by the F0 and F1 pin logic states. These pins include high-output drive capability for direct use of electromechanical counters and 2-phase stepper motors. Since this output supplies average active (real) power, any 2ω ripple on the output pulse period is minimal.

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4.0 DEVICE OVERVIEW

The MCP3905/06 is an energy-metering IC that supplies a frequency output proportional to active (real) power, and higher frequency output proportional to the instantaneous power for meter calibration. Both channels use 16-bit, second-order, delta-sigma ADCs that oversample the input at a frequency equal to MCLK/4, allowing for wide dynamic range input signals. A Programmable Gain Amplifier (PGA) increases the usable range on the current input channel (Channel 0). The calculation of the active (real) power, as well as the filtering associated with this calculation, is performed in the digital domain, ensuring better stability and drift performance. Figure 4-1 represents the simplified block diagram of the MCP3905/06, detailing its main signal-processing blocks.

Two digital high-pass filters cancel the system offset on both channels such that the real-power calculation does not include any circuit or system offset. After being high-pass filtered, the voltage and current signals are multiplied to give the instantaneous power signal. This signal does not contain the DC offset components, such that the averaging technique can be efficiently used to give the desired active (real) power output.

The instantaneous power signal contains the real-power information; it is the DC component of the instantaneous power. The averaging technique can be used with both sinusoidal and non-sinusoidal waveforms, as well as for all power factors. The instantaneous power is thus low-pass filtered in order to produce the instantaneous real-power signal.

A DTF converter accumulates the instantaneous active (real) power information to produce output pulses with a frequency proportional to the average active (real) power. The low-frequency pulses presented at the F_{OUT0} and F_{OUT1} outputs are designed to drive electro-mechanical counters and two-phase stepper motors displaying the real-power energy consumed. Each pulse corresponds to a fixed quantity of real energy, selected by the F2, F1 and F0 logic settings. The HF_{OUT} output has a higher frequency setting and lower integration period such that it can represent the instantaneous active (real) power signal. Due to the shorter accumulation time, it enables the user to proceed to faster calibration under steady load conditions (refer to **Section 4.7 "$F_{OUT0/1}$ and HF_{OUT} Output Frequencies"**).

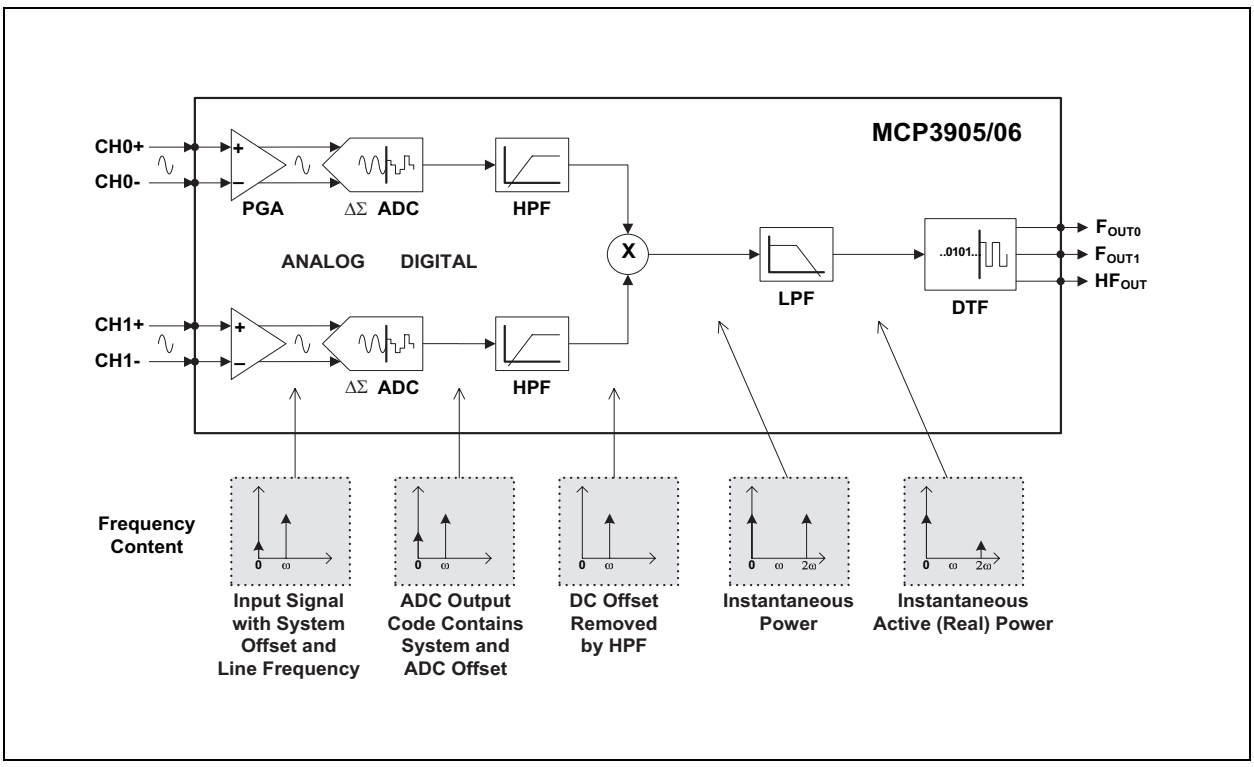


FIGURE 4-1: *Simplified MCP3905/06 Block Diagram with Frequency Contents.*

4.1 Analog Inputs

The MCP3905/06 analog inputs can be connected directly to the current and voltage transducers (such as shunts or current transformers). Each input pin is protected by specialized Electrostatic Discharge (ESD) structures that are certified to pass 5 kV HBM and 500V MM contact charge. These structures also allow up to ±6V continuous voltage to be present at their inputs without the risk of permanent damage.

Both channels have fully differential voltage inputs for better noise performance. The absolute voltage at each pin relative to A_{GND} should be maintained in the ±1V range during operation in order to ensure the measurement error performance. The common mode signals should be adapted to respect both the previous conditions and the differential input voltage range. For best performance, the common mode signals should be referenced to A_{GND}.

The current channel comprises a PGA on the front-end to allow for smaller signals to be measured without additional signal conditioning. The maximum differential voltage specified on Channel 0 is equal to ±470 mV/Gain (see Table 4-1). The maximum peak voltage specified on Channel 1 is equal to ±660 mV.

TABLE 4-1: MCP3905 GAIN SELECTIONS

G1	G0	CH0 Gain	Maximum CH0 Voltage
0	0	1	±470 mV
0	1	2	±235 mV
1	0	8	±60 mV
1	1	16	±30 mV

TABLE 4-2: MCP3906 GAIN SELECTIONS

G1	G0	CH0 Gain	Maximum CH0 Voltage
0	0	1	±470 mV
0	1	32	±15 mV
1	0	8	±60 mV
1	1	16	±30 mV

4.2 16-Bit Delta-Sigma ADCs

The ADCs used in the MCP3905/06 for both current and voltage channel measurements are delta-sigma ADCs. They comprise a second-order, delta-sigma modulator using a multi-bit DAC and a third-order SINC filter. The delta-sigma architecture is very appropriate for the applications targeted by the MCP3905, because it is a waveform-oriented converter architecture that can offer both high linearity and low distortion performance throughout a wide input dynamic range. It also creates minimal requirements for the anti-aliasing filter design. The multi-bit architecture used in the ADC minimizes quantization noise at the output of the converters without disturbing the linearity.

Both ADCs have a 16-bit resolution, allowing wide input dynamic range sensing. The oversampling ratio of both converters is 64. Both converters are continuously converting during normal operation. When the MCLR pin is low, both converters will be in Reset and output code 0x0000h. If the voltage at the inputs of the ADC is larger than the specified range, the linearity is no longer specified. However, the converters will continue to produce output codes until their saturation point is reached. The DC saturation point is around 700 mV for Channel 0 and 1V for Channel 1, using internal voltage reference.

The clocking signals for the ADCs are equally distributed between the two channels in order to minimize phase delays to less than 1 MCLK period (see **Section 3.2 "High-Pass Filter Input Logic Pin (HPF)"**). The SINC filters main notch is positioned at MCLK/256 (14 kHz with MCLK = 3.58 MHz), allowing the user to be able to measure wide harmonic content on either channel. The magnitude response of the SINC filter is shown in Figure 4-2.

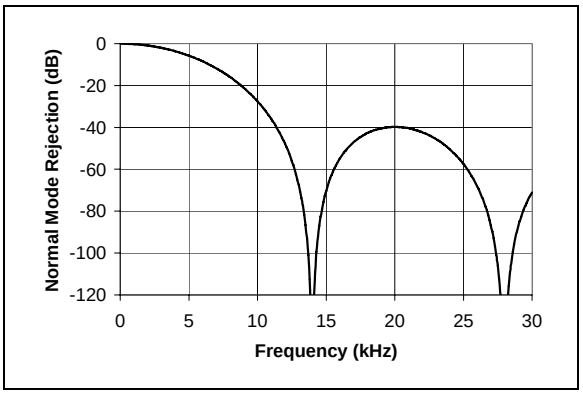


FIGURE 4-2: *SINC Filter Magnitude Response (MCLK = 3.58 MHz).*

4.3 Ultra-Low Drift V_{REF}

The MCP3905/06 contains an internal voltage reference source specially designed to minimize drift over temperature. This internal V_{REF} supplies reference voltage to both current and voltage channel ADCs. The typical value of this voltage reference is 2.4V, ±100 mV. The internal reference has a very low typical temperature coefficient of ±15 ppm/°C, allowing the output frequencies to have minimal variation with respect to temperature since they are proportional to $(1/V_{REF})^2$.

REFIN/OUT is the output pin for the voltage reference. Appropriate bypass capacitors must be connected to the REFIN/OUT pin for proper operation (see **Section 5.0 "Applications Information"**). The voltage reference source impedance is typically 4 kΩ, which enables this voltage reference to be overdriven by an external voltage reference source.

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If an external voltage reference source is connected to the REFIN/OUT pin, the external voltage will be used as the reference for both current and voltage channel ADCs. The voltage across the source resistor will then be the difference between the internal and external voltage. The allowed input range for the external voltage source goes from 2.2V to 2.6V for accurate measurement error. A V_{REF} value outside of this range will cause additional heating and power consumption due to the source resistor, which might affect measurement error.

4.4 Power-On Reset (POR)

The MCP3905/06 contains an internal POR circuit that monitors analog supply voltage AV_{DD} during operation. This circuit ensures correct device startup at system power-up/power-down events. The POR circuit has built-in hysteresis and a timer to give a high degree of immunity to potential ripple and noise on the power supplies, allowing proper settling of the power supply during power-up. A 0.1 µF decoupling capacitor should be mounted as close as possible to the AV_{DD} pin, providing additional transient immunity (see **Section 5.0 "Applications Information"**).

The threshold voltage is typically set at 4V, with a tolerance of about ±5%. If the supply voltage falls below this threshold, the MCP3905/06 will be held in a Reset condition (equivalent to applying logic '0' on the $\overline{\text{MCLR}}$ pin). The typical hysteresis value is approximately 200 mV in order to prevent glitches on the power supply.

Once a power-up event has occurred, an internal timer prevents the part from outputting any pulse for approximately 1s (with MCLK = 3.58 MHz), thereby preventing potential metastability due to intermittent resets caused by an unsettled regulated power supply. Figure 4-3 illustrates the different conditions for a power-up and a power-down event in the typical conditions.

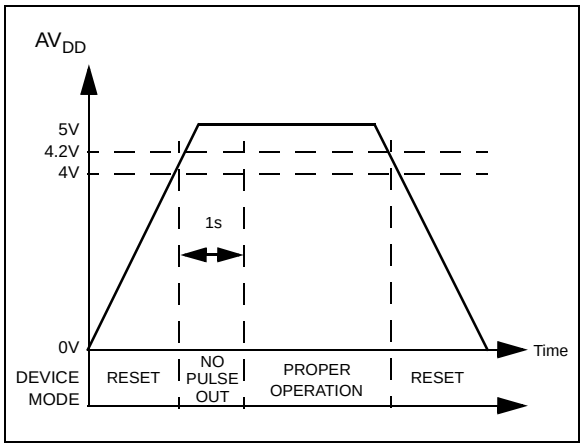


FIGURE 4-3: *Power-on Reset Operation.*

4.5 High-Pass Filters and Multiplier

The active (real) power value is extracted from the DC instantaneous power. Therefore, any DC offset component present on Channel 0 and Channel 1 affects the DC component of the instantaneous power and will cause the real-power calculation to be erroneous. In order to remove DC offset components from the instantaneous power signal, a high-pass filter has been introduced on each channel. Since the high-pass filtering introduces phase delay, identical high-pass filters are implemented on both channels. The filters are clocked by the same digital signal, ensuring a phase difference between the two channels of less than one MCLK period. Under typical conditions (MCLK = 3.58 MHz), this phase difference is less than 0.005°, with a line frequency of 50 Hz. The cut-off frequency of the filter (4.45 Hz) has been chosen to induce minimal gain error at typical line frequencies, allowing sufficient settling time for the desired applications. The two high-pass filters can be disabled by applying a logic '0' to the HPF pin.

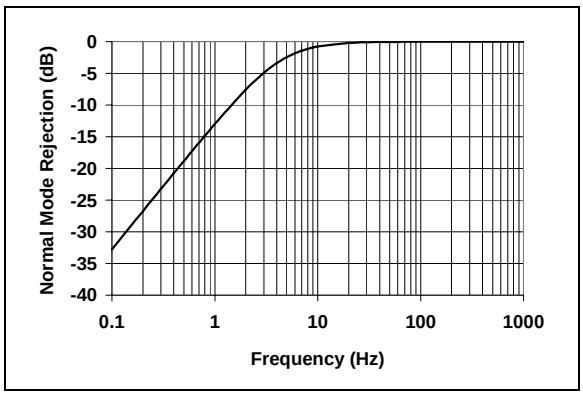


FIGURE 4-4: *HPF Magnitude Response (MCLK = 3.58 MHz).*

The multiplier output gives the product of the two high-pass-filtered channels, corresponding to instantaneous active (real) power. Multiplying two sine wave signals by the same ω frequency gives a DC component and a 2ω component. The instantaneous power signal contains the active (real) power of its DC component, while also containing 2ω components coming from the line frequency multiplication. These 2ω components come for the line frequency (and its harmonics) and must be removed in order to extract the real-power information. This is accomplished using the low-pass filter and DTF converter.

4.6 Low-Pass Filter and DTF Converter

The MCP3905/06 low-pass filter is a first-order IIR filter that extracts the active (real) power information (DC component) from the instantaneous power signal. The magnitude response of this filter is detailed in Figure 4-5. Due to the fact that the instantaneous power signal has harmonic content (coming from the 2ω components of the inputs), and since the filter is not ideal, there will be some ripple at the output of the low-pass filter at the harmonics of the line frequency.

The cut-off frequency of the filter (8.9 Hz) has been chosen to have sufficient rejection for commonly-used line frequencies (50 Hz and 60 Hz). With a standard input clock (MCLK = 3.58 MHz) and a 50 Hz line frequency, the rejection of the 2ω component (100 Hz) will be more than 20 dB. This equates to a 2ω component containing 10 times less power than the main DC component (i.e., the average active (real) power).

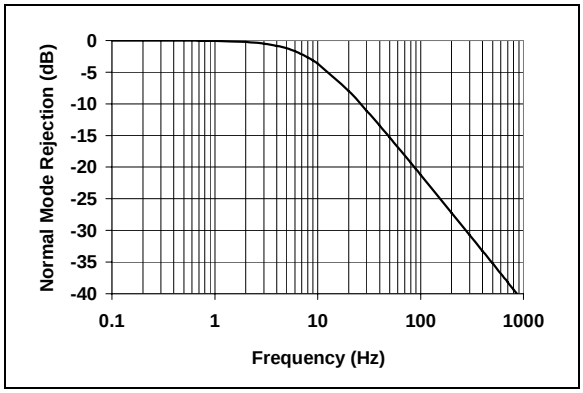


FIGURE 4-5: *LPF Magnitude Response (MCLK = 3.58 MHz).*

The output of the low-pass filter is accumulated in the DTF converter. This accumulation is compared to a different digital threshold for $F_{OUT0/1}$ and HF_{OUT}, representing a quantity of real energy measured by the part. Every time the digital threshold on $F_{OUT0/1}$ or HF_{OUT} is crossed, the part will output a pulse (See **Section 4.7 "$F_{OUT0/1}$ and HF_{OUT} Output Frequencies"**).

The equivalent quantity of real energy required to output a pulse is much larger for the $F_{OUT0/1}$ outputs than the HF_{OUT}. This is such that the integration period for the $F_{OUT0/1}$ outputs is much larger. This larger integration period acts as another low-pass filter so that the output ripple due to the 2ω components is minimal. However, these components are not totally removed, since realized low-pass filters are never ideal. This will create a small jitter in the output frequency. Averaging the output pulses with a counter or a Microcontroller Unit (MCU) in the application will then remove the small sinusoidal content of the output frequency and filter out the remaining 2ω ripple.

HF_{OUT} is intended to be used for calibration purposes due to its instantaneous power content. The shorter integration period of HF_{OUT} demands that the 2ω component be given more attention. Since a sinusoidal signal average is zero, averaging the HF_{OUT} signal in steady-state conditions will give the proper real energy value.

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4.7 $F_{OUT0/1}$ and HF_{OUT} Output Frequencies

The thresholds for the accumulated energy are different for $F_{OUT0/1}$ and HF_{OUT} (i.e., they have different transfer functions). The $F_{OUT0/1}$ allowed output frequencies are quite low in order to allow superior integration time (see **Section 4.6 "Low-Pass Filter and DTF Converter"**). The $F_{OUT0/1}$ output frequency can be calculated with the following equation:

EQUATION 4-1: F_{OUT} FREQUENCY OUTPUT EQUATION

$$F_{OUT}(Hz) = \frac{8.06 \times V_0 \times V_1 \times G \times F_C}{(V_{REF})^2}$$

Where:

- V_0 = the RMS differential voltage on Channel 0
- V_1 = the RMS differential voltage on Channel 1
- G = the PGA gain on Channel 0 (current channel)
- F_C = the frequency constant selected
- V_{REF} = the voltage reference

For a given DC input V, the DC and RMS values are equivalent. For a given AC input signal with peak-to-peak amplitude of V, the equivalent RMS value is V/sqrt(2), assuming purely sinusoidal signals. Note that since the active (real) power is the product of two RMS inputs, the output frequencies of an AC signal is half that of the DC equivalent signal, again assuming purely sinusoidal AC signals. The constant F_C depends on the F_{OUT0} and F_{OUT1} digital settings. Table 4-3 shows $F_{OUT0/1}$ output frequencies for the different logic settings.

TABLE 4-3: OUTPUT FREQUENCY CONSTANT FC FOR FOUT0/1 (V_{REF} = 2.4V)

F1	F0	F_C (Hz)	F_C (Hz) (MCLK = 3.58 MHz)	F_{OUT} Frequency (Hz) with Full-Scale DC Inputs	F_{OUT} Frequency (Hz) with Full-Scale AC Inputs
0	0	MCLK/2^{21}	1.71	0.74	0.37
0	1	MCLK/2^{20}	3.41	1.48	0.74
1	0	MCLK/2^{19}	6.83	2.96	1.48
1	1	MCLK/2^{18}	13.66	5.93	2.96

The high-frequency output HF_{OUT} has lower integration times and, thus, higher frequencies. The output frequency value can be calculated with the following equation:

EQUATION 4-2: HF_{OUT} FREQUENCY OUTPUT EQUATION

$$HF_{OUT}(Hz) = \frac{8.06 \times V_0 \times V_1 \times G \times HF_C}{(V_{REF})^2}$$

Where:

- V_0 = the RMS differential voltage on Channel 0
- V_1 = the RMS differential voltage on Channel 1
- G = the PGA gain on Channel 0 (current channel)
- F_C = the frequency constant selected
- V_{REF} = the voltage reference

The constant HF_C depends on the F_{OUT0} and F_{OUT1} digital settings with the Table 4-4.

The detailed timings of the output pulses are described in the Timing Characteristics table (see **Section 1.0 "Electrical Characteristics"** and Figure 1-1).

MINIMAL OUTPUT FREQUENCY FOR NO-LOAD THRESHOLD

The MCP3905/06 also includes, on each output frequency, a no-load threshold circuit that will eliminate any creep effects in the meter. The outputs will not show any pulse if the output frequency falls below the no-load threshold. The minimum output frequency on $F_{OUT0/1}$ and HF_{OUT} is equal to 0.0015% of the maximum output frequency (respectively F_C and HF_C) for each of the F2, F1 and F0 selections (see Table 4-3 and Table 4-4); except when F2, F1, F0 = 011. In this last configuration, the no-load threshold feature is disabled. The selection of F_C will determine the start-up current load. In order to respect the IEC standards requirements, the meter will have to be designed to allow start-up currents compatible with the standards by choosing the FC value matching these requirements. For additional applications information on no-load threshold, startup current and other meter design points, refer to AN994, *"IEC Compliant Active Energy Meter Design Using The MCP3905/6*", (DS00994).

TABLE 4-4: OUTPUT FREQUENCY CONSTANT HF_C FOR HF_{OUT} (V_{REF} = 2.4V)

F2	F1	F0	HF_C	HF_C (Hz)	HF_C (Hz) (MCLK = 3.58 MHz)	HF_{OUT} Frequency (Hz) with full-scale AC Inputs
0	0	0	64 x F_C	MCLK/2^{15}	109.25	27.21
0	0	1	32 x F_C	MCLK/2^{15}	109.25	27.21
0	1	0	16 x F_C	MCLK/2^{15}	109.25	27.21
0	1	1	2048 x F_C	MCLK/2^7	27968.75	6070.12
1	0	0	128 x F_C	MCLK/2^{16}	219.51	47.42
1	0	1	64 x F_C	MCLK/2^{16}	219.51	47.42
1	1	0	32 x F_C	MCLK/2^{16}	219.51	47.42
1	1	1	16 x F_C	MCLK/2^{16}	219.51	47.42

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5.0 APPLICATIONS INFORMATION

5.1 Meter Design using the MCP3905/06

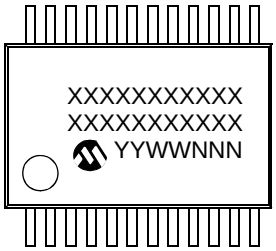
For all applications information, refer to AN994, *"IEC Compliant Active Energy Meter Design Using The MCP3905/6*" (DS00994). This application note includes all required energy meter design information, including the following:

- Meter rating and current sense choices
- Shunt design
- PGA selection
- F2, F1, F0 selection
- Meter calibration
- Anti-aliasing filter design
- Compensation for parasitic shunt inductance
- EMC design
- Power supply design
- No-load threshold
- Start-up current
- Accuracy testing results from MCP3905-based meter
- EMC testing results from MCP3905-based meter

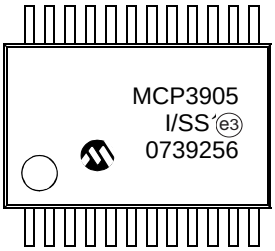
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

24-Lead SSOP



Examples:



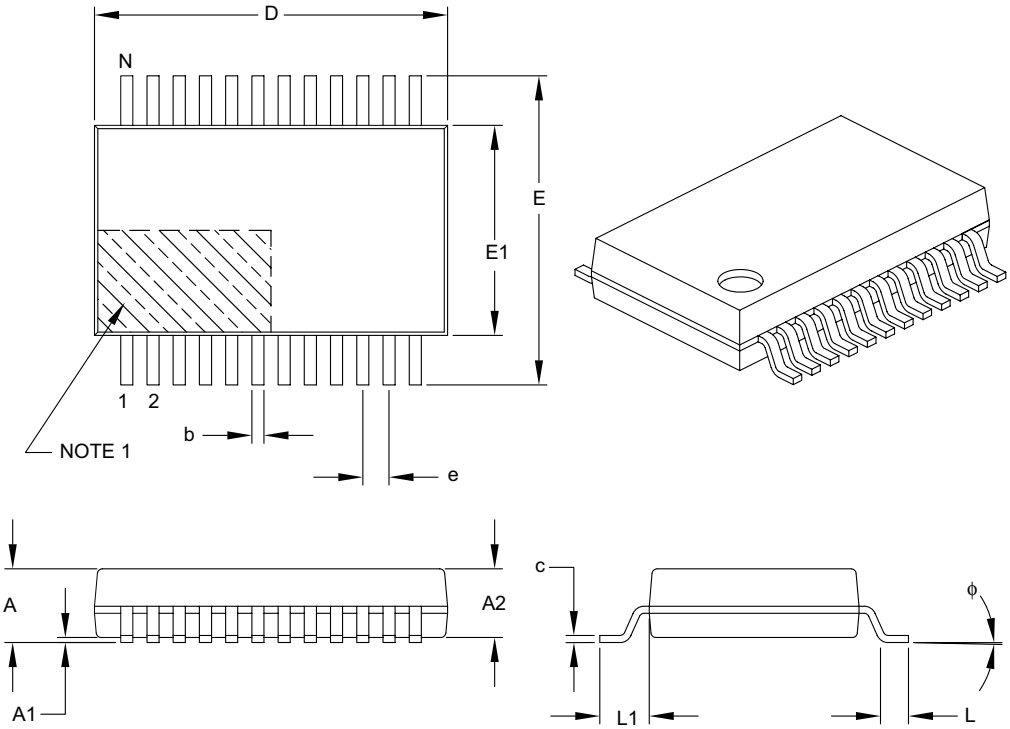
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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24-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		24	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	7.90	8.20	8.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-132B

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (July 2005)

Original Release of this Document.

Revision B (August 2005)

Replace Figures 2-1 thru 2-6 in **Section 2.0 "Typical Performance Curves"**

Revision C (October 2005)

Added references to MCP3905/06 throughout document.

Revision D (February 2007)

This revision includes updates to the packaging diagrams.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–X	/XX
Device	Temperature Range	Package

Device:	MCP3905:	Energy-Metering IC
	MCP3905T:	Energy-Metering IC (Tape and Reel)
	MCP3906:	Energy-Metering IC
	MCP3906T:	Energy-Metering IC (Tape and Reel)
Temperature Range:	I =	-40°C to +85°C
Package:	SS =	Plastic Shrink Small Outline (209 mil Body), 24-lead

Examples:

a) MCP3905-I/SS: Industrial Temperature, 24LD SSOP.

b) MCP3905T-I/SS: Tape and Reel, Industrial Temperature, 24LD SSOP.

a) MCP3906-I/SS: Industrial Temperature, 24LD SSOP.

b) MCP3906T-I/SS: Tape and Reel, Industrial Temperature, 24LD SSOP.

NOTES:

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Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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